This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS

1-6. (cancelled).

7. (previously presented) A method for simulating a system comprising a core in a microprocessor or a microcontroller and appertaining peripheral modules connected to the core, said method comprising the steps of:

in a first sequence of steps, simulating said microcontroller/microprocessor and said peripheral modules with predetermined signal patterns, said first sequence of steps having markers inserted therein;

in a second sequence of steps, interrogating and evaluating states of said system brought about by said simulation while executing said first sequence of steps, the second sequence of steps being executed by the core of the microprocessor or microcontroller for the system to be simulated; and

interrupting said first sequence of steps for executing said second sequence of steps as dictated by said markers inserted into said first sequence, said second sequence of steps being executed in an accelerated operational mode that is adapted to said evaluation.

8. (previously presented) The method as claimed in claim 7, wherein said first sequence of steps provides a clock-cycle-based simulation of said microcontroller/microprocessor and of said peripheral modules.

9. (previously presented) The method as claimed in claim 7, wherein said first sequence of steps is a series of consecutive program codes corresponding to program codes of at least one of the modules to be simulated.

10. (previously presented) The method as claimed in claim 9, wherein said markers are formed by one of opcodes or opcode sequences that are not usually used in said program code.

11. (previously presented) The method as claimed in claim 7, wherein peripheral modules that were specified during said second sequence of steps are functionally cosimulated.

12-13. (cancelled).

14. (previously presented) An apparatus for simulating a system comprising a core in a microprocessor or a microcontroller and appertaining peripheral modules connected to the core, the apparatus comprising:

a storage location for a first sequence of steps used to simulate the microcontroller/microprocessor and the peripheral modules with predetermined signal patterns, the first sequence of steps having markers inserted therein;

a storage location for a second sequence of steps used for interrogating and evaluating states of said system brought about by said simulation while executing said first sequence of steps, the second sequence of steps being executed by the core of the microprocessor or microcontroller for the system to be simulated upon interruption of said first sequence of steps for executing said second sequence of steps as dictated by said markers inserted into said first sequence, said second sequence of steps being executed in an accelerated operational mode that is adapted to said evaluation; and

a control unit for simulating the system by producing signal patterns that fundamentally have clock cycle accuracy and for evaluating the system states brought about by the simulation during a program interruption by activating an instruction set simulator.

15. (currently amended) The method as claimed in claim 7, wherein said first sequence of steps and said second sequence of steps are steps within the same software ~~present in a single peripheral~~ module.